IN THE CLAIMS:

1. A method of fabricating complementary bipolar transistors with SiGe base regions, comprising the steps

forming on a wafer a first collector region and a second collector region, each comprising an epitaxial layer of silicon;

and depositing a layer of silicon enhanced with germanium over each collector region in steps each separate from the other so that crystalline SiGe layers of differing germanium profiles materialize over said collector regions.

2. The method as set forth in claim 1 wherein

prior to a first step of the deposition of the layer of silicon enhanced with germanium over said collector regions, a continuous layer of silicon dioxide is deposited and over said layer of silicon dioxide a polycrystalline layer of silicon is deposited, after which said polycrystalline layer of silicon and said layer of silicon dioxide over said first collector region are removed;

the first step of the deposition of the layer of silicon enhanced with germanium is implemented so that a continuous layer of silicon enhanced with germanium is deposited that comprises a crystalline layer of SiGe formed over the epitaxial layer of silicon in said first collector region and a polycrystalline layer of SiGe formed over said polycrystalline layer of silicon; and

after which a continuous etch stop is deposited over said crystalline layer of SiGe and said polycrystalline layer of SiGe.

3. The method as set forth in claim 2 wherein

prior to a second step of the deposition of the layer of silicon enhanced with germanium over said second collector region, portions of said etch stop, said polycrystalline layer of SiGe and said polycrystalline layer of silicon as well as said layer of silicon dioxide are removed from over said second collector region;

the second step of deposition of said layer of silicon enhanced with germanium is implemented so that a continuous further layer of silicon is crystalline deposited, enhanced with germanium so that over said epitaxial layer of silicon in said second collector region said further layer of crystalline SiGe is formed and over said polycrystalline layer of SiGe a further layer of polycrystalline SiGe is formed;

after which a continuous resist is deposited; and

then said resist (38) and said further layer of polycrystalline SiGe are totally removed, said further layer of crystalline SiGe remaining over said second collector region.

4. The method as set forth in claim 3 wherein an in-situ doping of said further layer of crystalline SiGe occurs simultaneously with said deposition.

5. The method as set forth in claim 3 wherein doping said further layer of crystalline SiGe after deposition is done by ion implantation.

6. The method as set forth in claim 3 wherein said etch stop and said resist consist of silicon dioxide.

7. The method as set forth in claim 3 wherein in a region of said polycrystalline layer of SiGe outside of said collector regions a resistor is formed by implantation.

8. A method of fabricating complementary bipolar transistors with SiGe base regions, comprising the steps of:

forming a first collector region and a second collector region on a wafer, said first and second collector regions each comprising an epitaxial layer of silicon;

forming a first crystalline layer of SiGe over the first collector region; and

forming a second crystalline layer of SiGe over the second collector region such that the second crystalline layer of SiGe has a different germanium profile than the first crystalline layer of SiGe.

9. The method as set forth in claim 8, further comprising the steps of:

prior to the step of forming the first crystalline layer of SiGe, depositing a layer of silicon dioxide and depositing a polycrystalline layer of silicon over the layer of silicon dioxide;

then, removing portions of said polycrystalline layer of silicon and said layer of silicon dioxide over said first collector region;

wherein the first crystalline layer of SiGe is formed by depositing a first continuous layer of silicon enhanced with germanium such that said first crystalline layer of SiGe is formed over the epitaxial layer of silicon in said first collector region and a first polycrystalline layer of SiGe is formed over said polycrystalline layer of silicon; and

then, depositing a continuous etch stop over said first crystalline layer of SiGe and said first polycrystalline layer of SiGe.

10. The method as set forth in claim 9, further comprising the steps of:

prior to the step of forming the second crystalline layer of SiGe, removing portions of said etch stop, said first polycrystalline layer of SiGe, said polycrystalline layer of silicon, and said layer of silicon dioxide from over said second collector region;

wherein the second crystalline layer of SiGe is formed by depositing a second continuous layer of silicon enhanced with germanium such that said

second layer of crystalline SiGe is formed over the second collector region and a second polycrystalline layer of SiGe is formed over said first polycrystalline layer of SiGe;

after depositing the second layer of silicon enhanced with germanium, depositing a resist; and

then, removing said resist and said second layer of polycrystalline SiGe, wherein said second layer of crystalline SiGe remains over said second collector region.

11. The method as set forth in claim 10 wherein said second layer of crystalline SiGe is in-situ doped during deposition.

12. The method as set forth in claim 10, further comprising the step of doping said second layer of crystalline SiGe by ion implantation.

13. The method as set forth in claim 10 wherein said etch stop and said resist comprise silicon dioxide.

14. The method as set forth in claim 10 further comprising the step of forming a resistor by implantation into a region of said first polycrystalline layer of SiGe outside of said first and second collector regions.